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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,044	02/09/2004	Randall S. Mundt	AWS-040	8988

25199 7590 06/14/2005

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,044	MUNDT, RANDALL S.	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15 and 18-20* is/are rejected.

7)☒ Claim(s) *5,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *See Office Action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Information Disclosure Statement filed on 09/16/2004 is acknowledged by the examiner; A copy of a signed PTO-1449 attached with this office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-15 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Amazeen et al. (U.S. Patent 4,745,812).

Regarding claim 1:

Amazeen discloses a process tolerant sensor apparatus comprising:

a bottom substrate (fig. 8, unit 18); b) a top substrate (fig. 8, unit 12, 20); c) a plurality of sensors disposed between the bottom substrate and the top substrate (Col. 5-6, Lines 6-2);

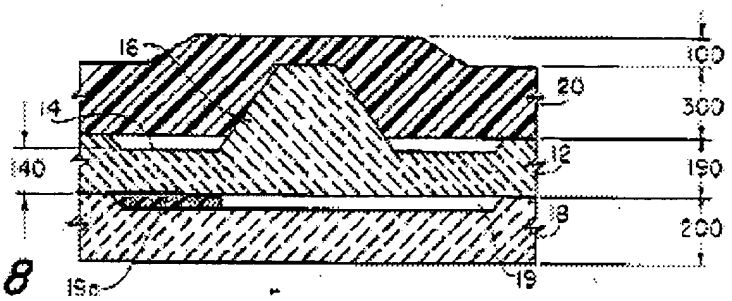


FIG. 8

d) a plurality of electrically conductive interconnects disposed between the bottom substrate and the top substrate (Col. 5-6, Lines 6-2); e) electrically active components connected to the conductive interconnects for at least one of data acquisition, data storage, and communications; and bonding material substantially filling the volume between the bottom substrate and the top substrate (Col. 6-7, Lines 3-32).

Regarding claim 18:

Amazeen discloses in a combination: a bottom semiconductor wafer (fig. 8, unit 18); a top semiconductor wafer (fig. 8, unit 12, 20); a plurality of sensors disposed between the bottom semiconductor wafer and the top semiconductor wafer (Col. 5-6, Lines 6-2);; a plurality of electrically conductive interconnects disposed between the bottom semiconductor wafer and the top semiconductor wafer (Col. 5-6, Lines 6-2); an electronics module comprising a housing containing electrically active components connected to the conductive interconnects for at least one of data acquisition, data storage (Col. 6-7, Lines 3-32), and comunication; and a bonding material substantially filling the volume between the bottom semiconductor wafer and the top semiconductor wafer (Col. 6-7, Lines 3-32).

Regarding claim 2, Amazeen discloses bottom substrate is a silicon wafer (Col. 5, Lines 51-59); Regarding claim 3, Amazeen discloses the top substrate is a silicon wafer (Col. 5, Lines 44-59); Regarding claim 4, Amazeen discloses top substrate is quartz (Col. 5, Lines 36-41); Regarding claim 7, Amazeen discloses

RF shielding material (Col. 5-6, Lines 60-2); Regarding claims 8, 15, Amazeen discloses shield electrically conductive layer (Col. 5-6, Lines 60-2); Regarding claim 9, Amazeen discloses shielding efficiency over predetermined frequency range (Col. 5-6, Lines 60-2); Regarding claim 10, Amazeen discloses at least one of the bottom substrate and the top substrate is thinned so that the thickness of the sensor apparatus substantially equals the thickness of a predetermined workpiece (fig. 8, unit 12, 18); Regarding claim 11, Amazeen discloses the plurality of sensors and electrically conductive interconnects are disposed upon the surface of the bottom substrate, a mirror image pattern of the sensors and interconnects is disposed upon the surface of the top substrate, and wherein the mirror image pattern and the sensors are of substantially the same thickness (fig. 8, unit 12, 18); Regarding claim 12, Amazeen discloses at least one of the electrically active components is disposed upon the surface of the bottom substrate, the top substrate has a hole, and the at least one of the electrically active components extends into the hole in the planar top substrate (fig. 8, unit 12 and 18); Regarding claim 13, Amazeen discloses the bottom substrate is electrically isolated from the top substrate (Col. 5, Lines 46-59); Regarding claim 14, Amazeen discloses the bottom substrate is electrically connected to the top substrate (Col. 5, Lines 46-59); Regarding claim 19, Amazeen discloses the top semiconductor wafer having a hole for receiving at least a portion of the electronics module (fig. 8, unit 12); Regarding claim 20, Amazeen discloses the top semiconductor wafer having a layer of

electromagnetic field shielding material (Col. 5-6, Lines 60-2); Regarding claim 6, the material is Epoxy (Col. 6, Lines 34-44).

Allowable Subject Matter

3. Claims 5, 17 and 16 re objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

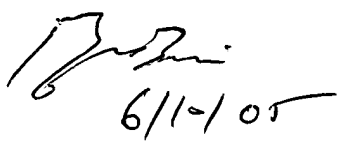
The following is an examiner's statement of reasons for allowance: prior art fail to teach: Regarding claim 5, the bonding material is between 0.05mm and 10mm; Regarding claim 16, the RF shielding material comprises at least one of a) an electrically conductive layer comprising at least one of silver, nickel, aluminum, and carbon, and b) a magnetically permeable film or layer comprising at least one of iron and cobalt; Regarding claim 17, the bottom substrate is selected from the group consisting of semiconductor wafer substrate, lithography mask substrate, printed circuit board substrate, and flat panel display substrate and the top substrate is selected from the group consisting of semiconductor wafer substrate, lithography mask substrate, printed circuit board substrate, and flat panel display substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should

preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRYAN BUI
PRIMARY EXAMINER



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